

USB4 2.0 ENGINEERING CHANGE NOTICE FORM

Title: Updating Sideband Register 12 on Asymmetric Transitions

Applied to: USB4 Specification Version 2.0

Brief description of the functional changes:

The Asymmetric Decision (TX/RX) should be updated when a dynamic Asymmetric Transition is initiated by the CM and not only on Lane Initialization.
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Benefits as a result of the changes:

These fields are used in Gen 4 Recovery flow and if their value doesn't match the current Link Width it might cause a change in the Link that was not intentional.
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An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
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None

An analysis of the hardware implications:
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None

An analysis of the software implications:
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None

An analysis of the compliance testing implications:
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None.

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Actual Change

(a). Table 4-20 – SB Register Fields

To Text:

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
12	Link Configuration	0	0	Enabling Decision (Lane 0) – Shall indicate whether the Lane 0 Adapter is enabled during Lane Initialization. 0b – Not enabled 1b – Enabled	RO	0b
			1	Enabling Decision (Lane 1) – Shall indicate whether the Lane 1 Adapter is enabled during Lane Initialization. 0b – Not enabled 1b – Enabled	RO	0b
			2	Asymmetric Decision (Tx) – Shall be set to 1b if both lanes are enabled and three transmitters are enabled in the USB4 Port, and shall be set to 0 otherwise. During Phase 3 in Lane Initialization, the value is based on Table 4-30, otherwise it is based on the Negotiated Link Width field. Shall be set to 1b if three transmitters are enabled in the USB4 Port, during Phase 3 in Lane Initialization, based on Table 4-30, otherwise based on the Negotiated Link Width field. Otherwise, shall be set to 0b. This bit shall only be set to 1b if both Lanes are enabled.	RO	0b
			3	Asymmetric Decision (Rx) – Shall be set to 1b if both lanes are enabled and three receivers are enabled in the USB4 Port, and shall be set to 0 otherwise. During Phase 3 in Lane Initialization, the value is based on Table 4-30, otherwise it is based on the Negotiated Link Width field. Shall be set to 1b if three receivers are enabled in the USB4 Port, during Phase 3 in Lane Initialization, based on Table 4-30 otherwise, based on the Negotiated Link Width field. Otherwise, shall be set to 0b. This bit shall only be set to 1b if both Lanes are enabled.	RO	0b